

Code No: 115EB**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD****B. Tech III Year I Semester Examinations, July/August - 2023****LINEAR AND DIGITAL IC APPLICATIONS****(Electronics and Communication Engineering)****Time: 3 Hours****Max. Marks: 75**

- Note:** i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A**(25 Marks)**

- 1.a) Mention the features of 723 regulators. [2]
- b) Write about comparator in brief. [3]
- c) What is all-pass filter? [2]
- d) What are the features of 555 timer? [3]
- e) How would you classify ADCs? [2]
- f) What is the drawback of weighted resistor DAC? Write down the method to overcome this drawback. [3]
- g) What is the magnitude comparator? [2]
- h) Write short notes about code converters. [3]
- i) Write the truth table for J-K flip-flop. [2]
- j) List out the applications of ROM. [3]

PART – B**(50 Marks)**

- 2.a) Explain the working of non-inverting amplifier and derive the equation of its Gain.
- b) Explain the working of an ideal and practical differentiator. [5+5]

OR

- 3.a) Explain the working of instrumentation amplifier with suitable diagram.
- b) What is an ideal active differentiator? Explain its working with neat circuit diagram. [5+5]

- 4.a) Design an active high pass filter with cutoff frequency of 4KHz.
- b) Draw and explain block schematic of PLL. [5+5]

OR

- 5.a) Explain the monostable multivibrator operation in IC 555 timer and derive its pulse width.
- b) Write about active notch filter. [7+3]

- 6.a) Explain about ladder type DAC with neat diagram.
- b) Draw the circuit and explain the working of dual slope A/D converter. [5+5]

OR

- 7.a) Explain the DAC and ADC specifications.
- b) Find the number of resistors required for an 8-bit weighted resistor D/A converter. Consider the smallest resistance is R and obtain those resistance values? [6+4]

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- 8.a) List out the merits and limitations of integrated circuit technology.
b) Give the design considerations of 2×4 decoder and explain the operation with relevant circuit. [5+5]

OR

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- 9.a) Implement the following Boolean function using 8:1 multiplexer
 $F(A,B,C,D) = \sum m(0,1,2,5,7,8,9,14,15)$
b) Design a 4 bit binary parallel subtractor and the explain operation in detail. [5+5]

- 10.a) Design a SR flip flop using NAND gates. Explain the operation of the SR flip flop with the help of characteristic table.
b) Describe shift registers and explain 4-bit bidirectional shift register with parallel load. [5+5]

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OR

- 11.a) Explain 4-bit synchronous up-down binary counter.
b) Discuss the read and write operations of SRAM. [5+5]

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